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	590 05/04/2006			Cer	tificate of Mailing or '	Transmission			
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DALLAS, TX 75252				Kristin R. Hayes Oppositors man		(Depositor's easist)			
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APPLICATION NO.	FILING DATE	<u> </u>	TRST NAMED INV		ATTORNEY DOCKET				
10/77,128 02/13/2004 Till Schloesser INF-135 3801 TITLE OF INVENTION: ARCHITECTURE FOR VERTICAL TRANSISTOR CELLS AND TRANSISTOR-CONTROLLED MEMORY CELLS									
APPLN. TYPE	SMALL ENTITY	LSSUE FEE		PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE			
nonprovisional	NO	\$0	_	\$0	\$0	08/04/2006			
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1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363). Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached. "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.			2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered attorney or agent) and the name is listed, no name will be printed.						
3. ASSIGNEE NAME AND		E DO INTER ON T	HE PATENT (pri	nt or type)					
2121222211122) RESIDENCE DATA TO E	E FAUNTED ON 1	PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filled for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filling an assignment.						
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Transmission Date:

July 31, 2006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:

Schloesser, et al.

Docket No.:

INF-135

Serial No:

10/777,128

Art Unit:

2818

Date Filed:

February 13, 2004

Examiner:

Andy Huynh

Title:

Architecture for Vertical Transistor Cells and Transistor-Controlled Memory

Cells

CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that the following papers are being transmitted by facsimile to the U.S. Patent and Trademark Office at (571) 273-2885 on the date shown above:

- Certification of Facsimile Transmission (1 page)
- Issue Fee Transmittal Letter (1 page)
- Part B Fee(s) Transmittal (2 duplicate pages)

Respectfully submitted,

Kristin R. Haves Legal Assistant

Confirmation Respectfully Requested

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Title:

Architecture for Vertical Transistor Cells and Transistor-Controlled Memory

Cells

Mail Stop: Issue Fee Commissioner of Patents P. O. Box 1450 Alexandria, VA 22313-1450

ISSUE FEE TRANSMITTAL LETTER

Dear Sir:

A Notice of Allowance dated May 4, 2006 indicating the allowance of the pending claims in the above application was issued in this case. Applicant has previously paid the issue fee and requests that such previous payment be applied towards the newly required issue fee payment. Additionally, the Commissioner is hereby authorized to charge and additional fees or credit any overpayments to Deposit Account No. 50-1065.

Respectfully submitted,

Ira S. Matsil

Attorney for Applicant

Reg. No. 35,272

Slater & Matsil, L.L.P. 17950 Preston Road, Suite 1000 Dallas, TX 75252 (972) 732-1001 (telephone) (972) 732-9218 (facsimile)